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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Application Number	10/63703
			Filing Date	Concurrently Herewith 7/7/03
			First Named Inventor	Fuaida Harun
			Group Art Unit	2896
			Examiner Name	William S
Sheet	1	of	Attorney Docket Number	SC12793MP

U. S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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AA	AA	Ker <i>et al.</i> , "Design on the Low-Capacitance Bond Pad for High-Frequency I/O Circuits in CMOS Technology," <i>IEEE Transactions on Electron Devices</i> , Vol. 48, No. 12, December 2001, pp. 2953-2956.	

Examiner Signature		Date Considered	4/18/05
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